

XSCC: A High-Performance Compiler for RISC-V



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XSCC Team Overview

Technical Expertise

Strong expertise spanning compiler research and development

2001



ORC



Loongson-2
Compiler



SWCC



Loongson-3
Compiler

so far



XSCC

- Test-of-Time Award at CGO 2021
- Best Paper Award at ASE 2019
- Publications at top-tier international conferences, including OSDI, SC, MICRO and ASPLOS
- Finalist for the Gordon Bell Prize twice

XSCC: Hardware/Software Co-Design



中科院计算所

INSTITUTE OF COMPUTING TECHNOLOGY, CAS



北京开源芯片研究院
BEIJING INSTITUTE OF OPEN SOURCE CHIP



山东科技大学

SHANDONG UNIVERSITY OF SCIENCE AND TECHNOLOGY



哈尔滨工程大学

HARBIN ENGINEERING UNIVERSITY



西华师范大学

CHINA WEST NORMAL UNIVERSITY

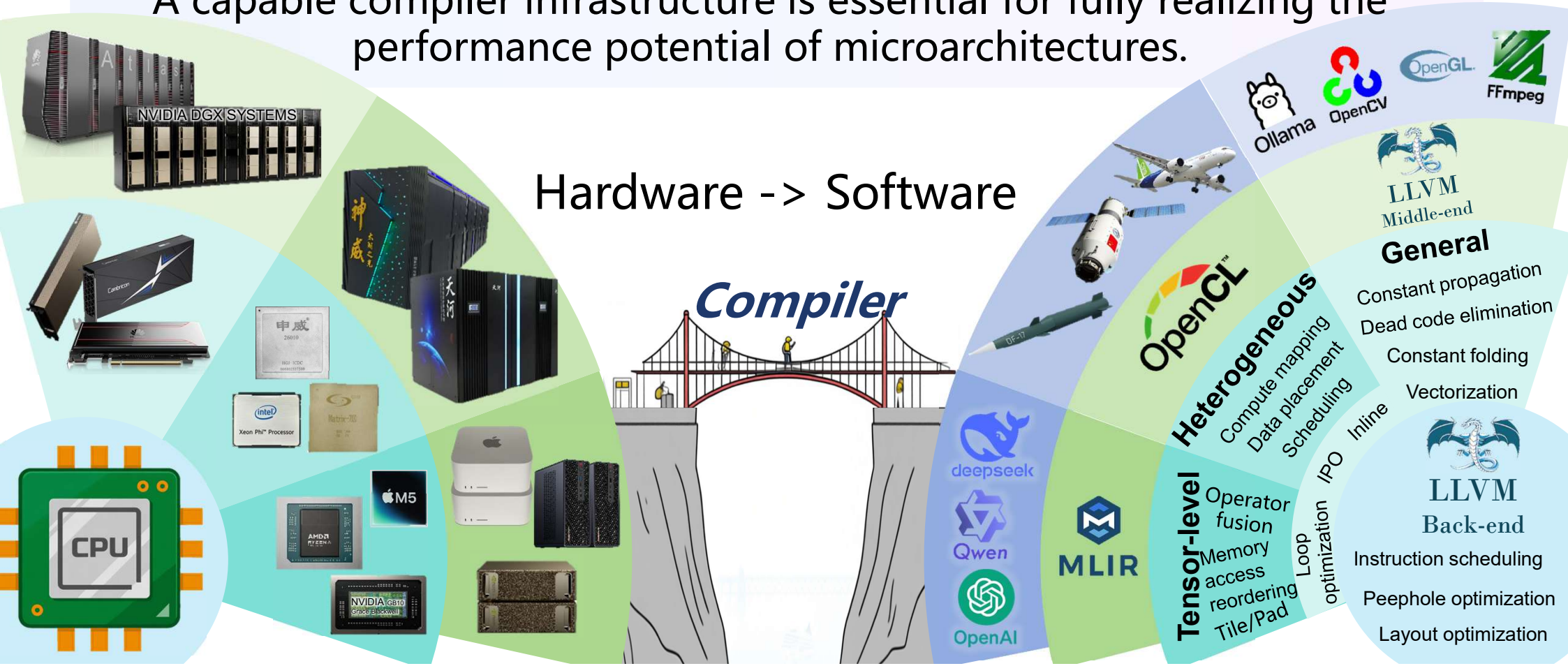
XSCC Team Overview



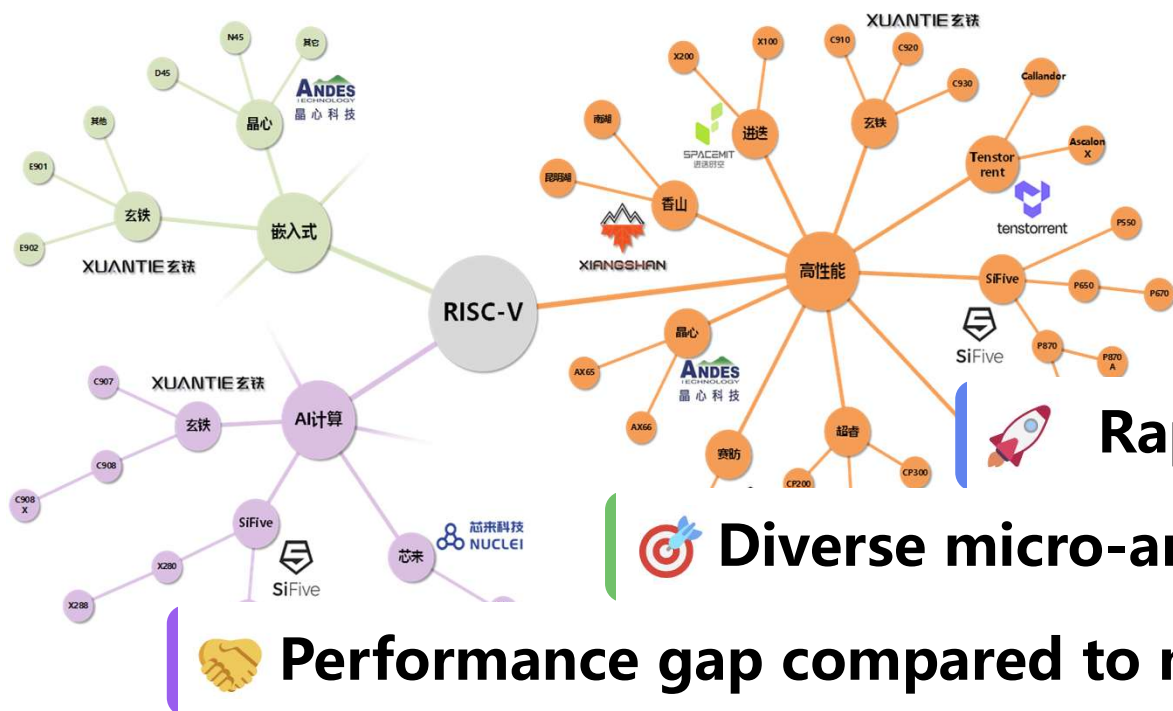
Motivation: Why Compilers Matter

Compiler: programming language -> machine code

A capable compiler infrastructure is essential for fully realizing the performance potential of microarchitectures.



Challenges for RISC-V Compilers



Rapidly evolving ISA extensions

Diverse micro-architectural implementations

Performance gap compared to mature ecosystems (e.g., x86, Arm)

High-Performance Compiler for RISC-V

XSCC: A High-Performance Compiler for RISC-V



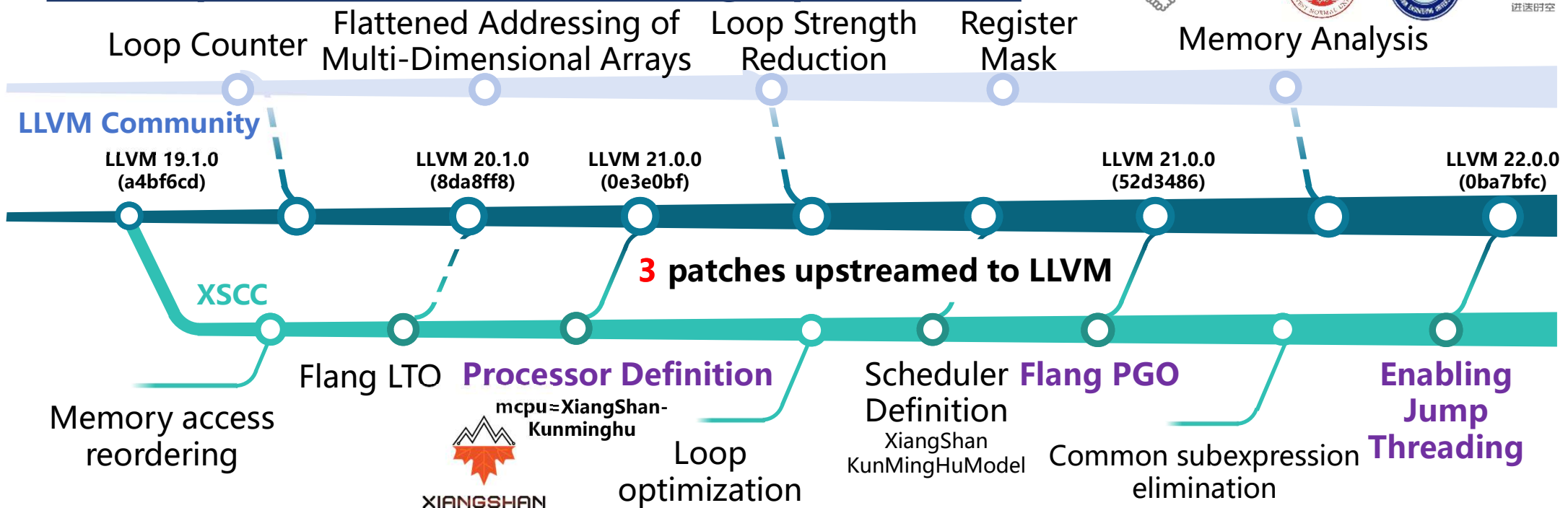
XSCC is designed to serve

- ✓ Industrial-grade performance needs
- ✓ Open-source ecosystem development
- ✓ Competitive performance
- ✓ Engineering robustness
- ✓ Deep integration with the RISC-V ecosystem

Core Goals

From Open Source, and Benefiting Open Source

Acknowledgements



Excellent Performance Across RISC-V Microarchitectures

KMHv3 GEM5 @3GHz *Date: Mon Oct 27 16:46:57 2025 +0800

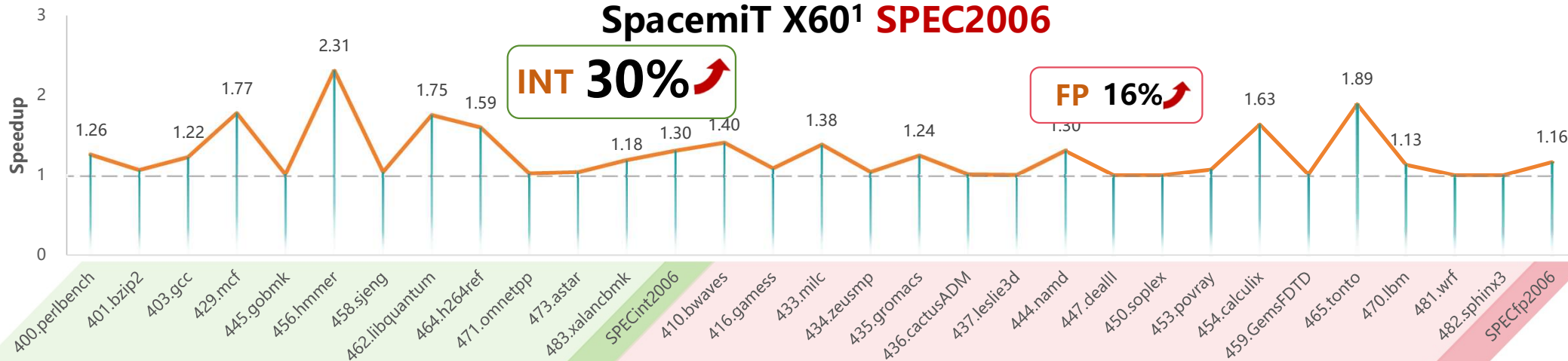
Base: INT 21.13 (↑8%) ; FP 22.27 (↑12%) Peak: INT 22.11 (↑13%) ; FP 22.63 (↑14%)

SPEC06INT	LLVM19	GCC12	XSCC1.0	XSCC1.0	SPEC06FP	LLVM19	GCC12	XSCC1.0	XSCC1.0
	base-scalar	base-scalar	base-scalar	peak-scalar		base-scalar	base-scalar	base-scalar	peak-scalar
400.perlbench	17.54	16.83	17.10	18.16	416.gamess	17.94	16.77	18.44	18.22
401.bzip2	9.98	9.93	10.07	10.35	433.milc	25.35	22.39	32.60	30.15
403.gcc	15.64	21.05	15.61	21.82	434.zeusmp	22.01	24.25	22.05	22.71
429.mcf	29.14	32.00	30.78	31.81	435.gromacs	13.82	15.65	14.22	14.06
445.gobmk	15.67	15.81	15.93	15.66	436.cactusADM	27.87	20.17	29.14	30.31
456.hmmer	18.03	15.43	17.31	22.61	437.leslie3d	24.15	23.76	24.43	24.59
458.sjeng	14.51	12.73	14.56	14.43	444.namd	14.47	12.40	14.45	14.50
462.libquantum	48.69	46.75	113.99	102.47	447.dealll	30.57	30.44	33.27	30.24
464.h264ref	24.89	24.40	25.24	25.45	450.soplex	22.65	23.35	22.78	23.63
471.omnetpp	19.31	21.02	19.39	19.95	453.povray	23.48	23.70	24.18	23.74
473.astar	12.40	12.49	12.36	14.90	454.calculix	7.24	6.69	14.08	21.43
483.xalancbmk	32.36	32.62	34.54	26.43	459.GemsFDTD	23.02	18.63	26.30	26.28
SPECint2006	19.53	19.70	21.13	22.11	465.tonto	7.18	14.87	11.43	11.28
					470.lbm	52.43	36.50	52.63	51.98
					481.wrf	16.45	18.63	15.56	15.33
					482.sphinx3	19.21	17.96	19.37	19.16
					SPECfp2006	19.88	19.69	22.27	22.63

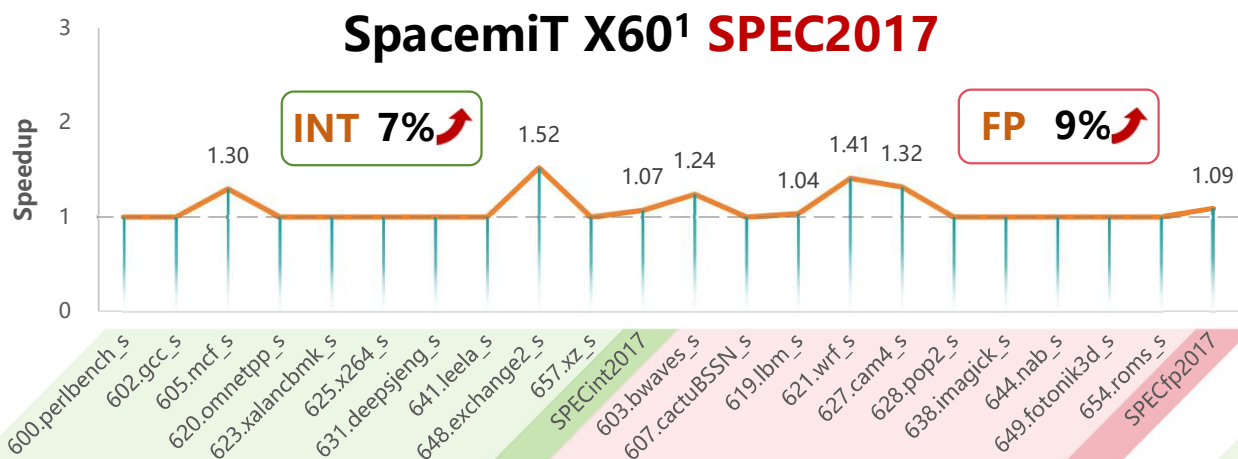
xsc: https://somsubhra.github.io/github-release-stats/?username=OpenXiangShan&repository=xsc&page=1&per_page=5

Excellent Performance Across RISC-V Microarchitectures

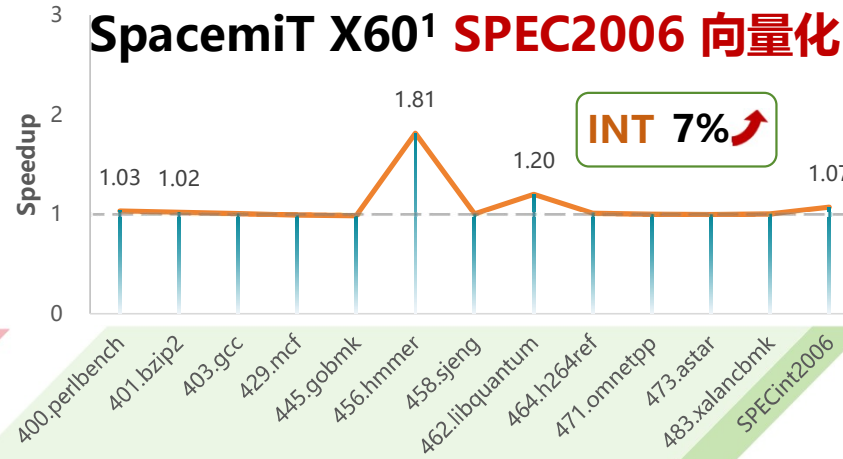
SpacemiT X60¹ SPEC2006



SpacemiT X60¹ SPEC2017



SpacemiT X60¹ SPEC2006 向量化



¹ SpacemiT Muse Pi with M1 Core 1.6GHz RV64GCBV 16GB RAM

Binary Release

https://somsubhra.github.io/github-release-stats/?username=OpenXiangShan&repository=xsc&page=1&per_page=5

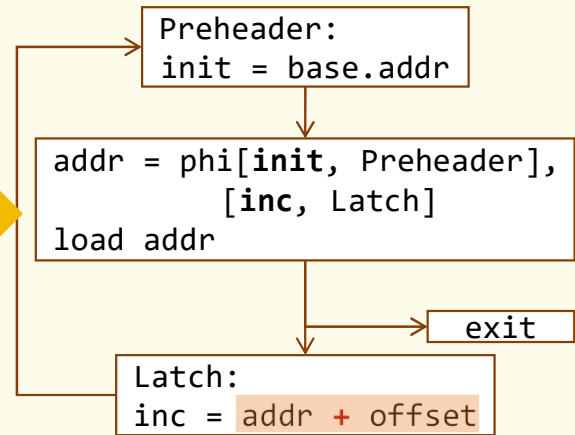
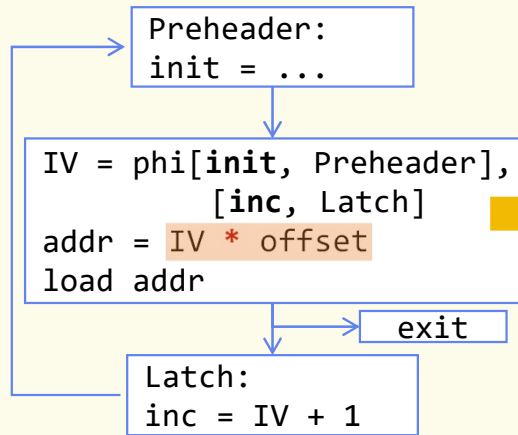
Why XSCC Performs Well

Transferring Cross-Architecture Optimization Experience to RISC-V



Representative Example

648.exchange2_s

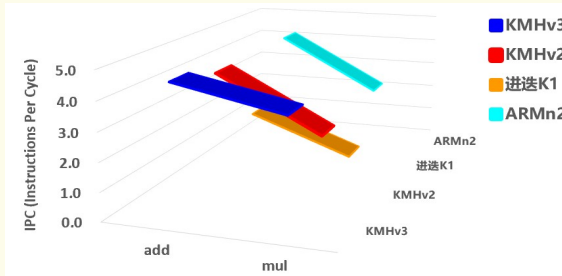


LLVM Weekly - #603, July 21st 2025

Community Newsletters llvm-weekly

- "Leilongjie2000" started an RFC discussion on [missed LoopStrengthReduce opportunities for outer loops containing inner loops](#) 1, including the SPEC CPU 2017 648.exchange2_s benchmark.

Feedback to LLVM community



进迭K1 ratio speedup

	ratio	speedup
LLVM	1.84	—
XSCC	2.23	1.21x

Thanks!

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